Amendments to the Claims

1-18. (Canceled).

19. (currently amended) A current mirror circuit, comprising:

a reference current side having a first transistor and a second transistor, a source of said first transistor coupled to a drain of said second transistor; and

a load current side having a third transistor, a gate of said third transistor connected to a gate of said second transistor, a drain of said third transistor connected to a load circuit;

wherein a drain-to-source voltage drop across said second transistor matches a drain-to-source voltage drop across said third transistor;

wherein a voltage is applied to a gate of said first transistor, said voltage based on a common mode voltage associated with an input of said load circuit.

20. (original) The current mirror circuit of claim 19, wherein a reference current in said reference current side tracks changes of a load current in said load current side.

21. (original) The current mirror of claim 20, wherein said reference current is scaled relative to said load current.

22. (original) A current mirror circuit, comprising:

a reference current side having a first transistor and a second transistor, a source of said first transistor coupled to a drain of said second transistor; and

a load current side having a third transistor, a gate of said third transistor connected to a gate of said second transistor, a drain of said third transistor connected to a load circuit;

wherein said load current side supplies a load current to said load circuit, and said reference current side generates a reference current that is proportional to said load current so that said reference current tracks changes in said load current;

wherein a voltage is applied to a gate of said first transistor, said voltage based on a common mode voltage associated with an input of said load circuit.

23. (original) A method for maintaining a current ratio in a current mirror circuit, the current mirror having a reference current side with a first transistor coupled to a second transistor, and a load current side having a third transistor with a gate connected to a gate of the second transistor, comprising:

generating a reference current in the reference current side;

generating a load current in the load current side that is proportional to the reference current generated in the reference current side; [[and]]

causing a drain-to-source voltage drop across said second transistor to match a drain-to-source voltage drop across said third transistor so that said reference current tracks changes in said load current;

applying a voltage to a gate of said first transistor, wherein said voltage is based on a common mode voltage associated with an input of said load circuit .

24. (new) The current mirror of claim 19, wherein said source of said first transistor is coupled to said drain of said second transistor though a resistor.

25. (new) The current mirror of claim 24, wherein said resistor is determined based on an impedance of said load circuit.

26. (new) The current mirror of claim 19, wherein said load circuit includes a differential input having said common mode voltage that is an average of said differential input.

27. (new) The current mirror of claim 22, wherein said source of said first transistor is coupled to said drain of said second transistor though a resistor.

28. (new) The current mirror of claim 27, wherein said resistor is determined based on an impedance of said load circuit.

29. (new) The current mirror of claim 22, wherein said load circuit includes a differential input having said common mode voltage that is an average of said differential input.